WHAT IS CLAIMED IS:

1. A protocol structure to accelerate memory transmission, and the features including: a built-in address memory unit located in front end of the memory, of which comprises several address buffers, and there is a pointing design between each address buffer and the corresponding data block in the memory;

The several address buffers located in the aforementioned memory address unit provide the external pins to enter address data in advance and further to select quickly the corresponding data block that an address buffer points to so as to rapidly change the data address for data transmission and access.